CLAIMS

What is claimed:

1. A memory cell comprising:

two electrodes;

a polymeric body, between the electrodes, having a plurality of roughness formations on a surface thereof, the roughness formations having a height, the polymeric body maintaining a charge after a voltage is applied across the electrodes; and

an interface material, between at least one of the electrodes and the surface of the polymeric body, having a thickness being greater than the height of the roughness formations.

2. The memory cell of claim 1, wherein the polymeric body maintains a second charge after a second voltage is applied across the electrodes.

3. The memory cell of claim 2, wherein the interface material completely separates the at least one electrode and the polymeric body.

4. The memory cell of claim 3, wherein the thickness of the interface material is at least 150 angstroms.

5. The memory cell of claim 4, wherein the electrodes are metal.

6. The memory cell of claim 5, wherein the electrodes are made of at least one of titanium nitride, titanium, and aluminum.

7. The memory cell of claim 6, wherein the polymeric body is ferroelectric.

8. The memory cell of claim 7, wherein the polymeric body includes fluorine.

9. The memory cell of claim 8, wherein the height of the roughness formation is between 600 and 1000 angstroms.

10. The memory cell of claim 6, wherein the interface material is titanium oxide.

11. A semiconductor device comprising;

a substrate;

a first layer, on the substrate, having a plurality of first conductive lines therein;

a second layer, on the first layer, having a plurality of polymeric sections, each polymeric section being over at least a portion of at least one of the first conductive lines, the polymeric sections having a plurality of

roughness formations on a surface thereof, the roughness formations having a height;

a third layer, on the second layer, having a plurality of interface sections, each interface section being adjacent to at least one of the polymeric sections, each interface section having a thickness greater than the height of the roughness formations; and

a fourth layer, on the third layer, having a plurality of second conductive lines therein, each second conductive line extending over at least one first conductive line, at least one polymeric section, and at least one interface section to form a plurality of memory cells such that a voltage applied across one of the first conductive lines and one of the second conductive lines changes a charge of the polymeric section from a first value to a second value.

12. The semiconductor device of claim 11, wherein the thickness of each interface section is at least 150 angstroms.

13. The semiconductor device of claim 12, wherein the substrate is silicon and has mircoelectronic circuitry formed therein.

14. The semiconductor device of claim 13, further comprising an insulating layer between the substrate and the first layer.

15. The semiconductor device of claim 14, wherein the insulating layer is silicon oxide.

16. The semiconductor device of claim 15, wherein the first and second conductive lines are made of at least one of titanium nitride, titanium, and aluminum.

17. The semiconductor device of claim 16, wherein the polymeric sections are ferroelectric.

18. The semiconductor device of claim 17, wherein the height of the roughness formations is between 600 and 1000 angstroms.

19. The semiconductor device of claim 18, wherein the interface sections are made of titanium oxide.

20. The semiconductor device of claim 19, wherein said layers are stacked vertically.

21. A method for constructing a memory cell comprising:

forming a polymeric body on a first electrode, the polymeric body having a plurality of roughness formations on a surface thereof, the roughness formations having a height;

depositing an interface material on the surface of the polymeric body, the interface material having a thickness greater than the height of the roughness formations; and

forming a second electrode on the interface material to change a charge of the polymeric body from a first value to a second value when a voltage is applied across the first electrode and the second electrode.

22. The method of claim 21, wherein the thickness of the interface material is at least 150 angstroms.

23. The method of claim 22, further comprising forming the first electrode on a substrate.

24. The method of claim 23, wherein the polymeric body is ferroelectric.

25. A method for constructing a semiconductor device comprising:

forming a dielectric layer on a substrate;

forming a plurality of first conductive lines, extending in a first direction, on the dielectric layer;

forming a plurality of polymeric sections on the first conductive lines, the polymeric sections having a plurality of roughness formations on surface thereof, the roughness formations having a height;

forming a plurality of interface sections on the polymeric sections, the interface sections having a thickness greater than the height of the roughness formations; and

forming a plurality of second conductive lines, extending in a second direction, on the interface sections to position each respective pair of polymeric and interface sections between one first and second conductive line, the second direction being transverse to the first direction.

26. The method of claim 25, wherein the thickness of the interface sections is at least 150 angstroms.

27. The method of claim 26, wherein the interface sections are titanium oxide.

28. The method of claim 27, wherein the conductive lines are made of at least one of titanium nitride, titanium, and aluminum.

29. The method of claim 28, wherein the second direction is substantially perpendicular to the first direction.

30. The method of claim 29, wherein said formation of polymeric sections comprises spinning a polymeric layer onto the substrate and curing the polymeric layer.